

T7 DPU Products

High Performance Programmable DPU 1/10/25/40/50/100/200/400GbE Controller

Enables several offloads, programmable compute, encryption, FPGA integration, virtualization over a single wire.

Highlights

- Full suite of Storage features
- Full suite of Cloud features
- Full suite of data center networking features
- Full suite of data streaming features
- Full suite of encryption functions
- Embedded programmable DPU
- Embedded Arm A72 cores, accessible by user
- Adapter or micro-server functionality
- Ability to integrate with an external FPGA
- Integrated Ethernet and PCle switch
- Software Compatible with T4, T5, and T6

Applications

Datacenter Networking

- Scale out servers and NAS systems
- Consolidate LAN, SAN, and cluster networks (run InfiniBand and Fibre Channel applications on Ethernet)
- Enhanced network and server security

Cloud Computing

- Virtualization features to maximize cloud scaling and utilization
- Cloud-ready functional and management features
- Secure Sockets offload
- Full support for overlay products
- Seamless integration with external FPGA

Networked Storage

- Develop high-performance shared-storage systems providing both file and block level services
- Computational Storage
- Ethernet to the Drive
- Integrated encryption support
- NVMe Fabrics (iWARP & RoCEv2)
- NVMe/TCP (including NVMe offload)
- Very high data-integrity
- Dedupe, Compression support
- RAID, Erasure Coding support

High Performance Computing

- Very low latency Ethernet
- High performance RDMA support
- Increase cluster fabric bandwidth

Streaming Applications

- Internet attack protection
- QoS and Traffic Management
- Video streaming

Edge Products

- Micro Servers
- Gateways
- 5G Appliances
- Firewalls

Overview

Chelsio's T7 is a quad port 1/10/25/50/100Gb, dual port 40/100/200Gb, or single port 400Gb Ethernet Unified Wire DPU ASIC with a PCI Express 5.0 host bus interface, optimized for storage, cloud computing, HPC, embedded, virtualization, security, AI, and other datacenter networking applications.

The seventh generation T7 ASIC technology from Chelsio provides the highest performance and efficiency, with dramatically lower host system CPU communications overhead. Thanks to on-board

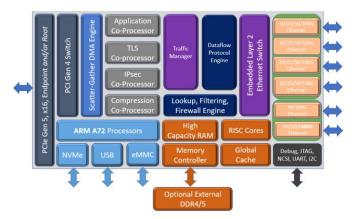


hardware, that offloads TCP/IP, UDP/IP, Unified RDMA (RoCEv2 & iWARP), iSCSI, NVMe-oF, NVMe/TCP, NVGRE, VXLAN, and TLS/IPsec processing from its host system and frees up host CPU cycles for user applications. As a result, the system benefits from higher bandwidth, lower latency, and reduced power consumption.

T7 runs the predecessor T4, T5, & T6 silicon software without modification to enable leveraging of the user's existing software investment. T7's architecture is Chelsio's 7th generation DPU technology road-tested across several tier-1 OEMs over the years and has evolved to support all offloads using either card memory or host memory. As a result, T7 technology can now enable a full featured DPU technology in a small memory-free package to address server and cloud applications at an aggressive price point.

The Smart NIC Programmable DPU Solution

In addition to the above offloads, versions of T7 integrate 8 A72 Arm cores that are exposed to the user. These Arm cores offload the traffic to the integrated 400Gb DPU on the chip and as a result the Arm cores are available to support the user's specific application. The T7 transport engine is a programmable DPU that can offload protocol processing per connection, per-server, per-interface, while simultaneously providing complete stateless offload to traffic for non-offloaded connections (processed by operating systems stack running on host CPU). The T7 also provides a flexible direct data placement capability for regular TCP sockets, with all the benefits of zero-copy and kernel bypass without rewriting the applications. To support the Arm Cores, Chelsio provides a full development and debug software package to allow development of application specific firmware.



T7 Block Diagram

Features

	T7 N7		T7	N7		T7 N
Host Interface		Storage			TCP & UDP Offload	
PCI Express Gen5 x16	~ ~	iSCSI initiator and target mode stack	v	~	Full TCP stack including IPv4 & IPv6	~ ~
End Point (EP) operation	~ ~	T10 DIF/DIX support for iSCSI	~	~	Extensive RFC compliance, fully featured	~ ~
Root Complex (RC) operation	✓	NVMe-oF Offload (iWARP)	~	•	VLAN support up to 4096 VLAN IDs	<i>y y</i>
Concurrent RC+EP (NVMe-NVMe Bridge)	✓	NVMe-oF Offload (RoCEv2)	~	•	Load balancing and failover capabilities	•
Integrated PCIe Gen4 Switch	✓	NVMe/TCP Offload	~	•	UDP Sockets API	•
MSI-X, MSI, legacy pin interrupts	, ,	QUIC Offload	~	~	Low user-to-user latency	<i>y y</i>
		Dedupe offload	~		Multicast replication on ingress or egress	•
Wire Interface		Erasure Code offload	~		Patented Seamless Failover	<i>y y</i>
NRZ or PAM4	y y	RAID 5/6 offload	~		Proxy Switching	•
4x1/10/25/50/100G or 2x40/100/200G or 1x400G	, ,	Compression (LZ77+Huffman, Gzip, XP10, zlib)	•		High capacity offload without card memory	, ,
IEEE 802.3cd (50/100/200GbE)	~ ~	Decompression (LZ77+Huffman, Gzip, XP10, zlib)	~			
IEEE 802.3bs 200GbE	, ,	PMoF	V		Data Center Features	
IEEE 802.3by 25GbE	, ,	iSER	~	~	Internet Attack Protection	, ,
IEEE 802.3bm 40GbE/100GbE	y y	Data-at-rest encryption	~	•	PFC, DCB, CEE	, ,
IEEE 802.3ba (40/100GbE)	y y	,,			Time stamping support	, ,
IEEE 802.3bj (100 GbE over copper/backplane)	, ,	Security			Flow mirroring, sampling and statistics	<i>y y</i>
IEEE 802.3az Energy Efficient Ethernet	y y	AES 128/256 and SHA1/SHA2 offload	~	v	GPUDirect	, ,
IEEE 802.3ap Backplane Ethernet	, ,	TLS and IPsec co-processor mode	_	,	GPUDirect Storage (GDS)	, ,
IEEE 802.3ae (10 GbE)	, ,	TLS and IPsec inline mode	,	J		
IEEE 802.3z (1GbE)	, ,	QUIC co-processor mode	_	,	Embedded Processors	
IEEE 802.1p Priority	, ,	QUIC inline mode	,	J	ARM A72 Cores (1.5 GHz), 2MB L2 Cache	~
IEEE 802.1Q VLAN Tagging	, ,	SM2, RSA, ECC, ECDH, ECDSA, DSA, DH	,		ARM API (IPDK)	•
IEEE 802.1Qbg EVB/VEPA	, ,	Inline IPsec & TLS for all Offload Traffic	,	v	400Gb DPU Core	,
IEEE 802.1BR Bridge Port Extension	, ,	True Random Number Generator	,		Dual-Channel 4800MT/s DDR5	, ,
IEEE 802.1Qau Congestion Notification	· ·	Secure firmware update	,	V	244. 6.14	
IEEE 802.1Qbb PFC	, ,	Hardware Root of Trust support	J	J	Management and Other Interfaces	
IEEE 802.1Qaz (ETS)	, ,				USB 2.0 Host Mode	v
IEEE 802.3x Flow Control	, ,	Cloud & Virtualization			USB 2.0 Target Mode	Ţ
IEEE 802.3ad Load-balancing and Failover	, ,	NVMe Virtualization/Emulation	_		UART	,
Ethernet II and 802.3 encapsulated frames	, ,	Virt-IO	,		eMMC 4.51	
Multiple MAC addresses per interface	, ,	OVS Offload	,		NVMe Gen 4, x2	J
Jumbo Frames up to 9.6 Kbytes	, ,	Seamless integration with external FPGA	,		NC-SI	,
ITU-T G.8262, Sync-E	· ·	Inband Telemetry	,	V	SPI Flash	,
IEEE 802.1AS Timing and Synchronization	, ,	NVGRE, VXLAN and GENEVE support	,	J	I2C, MDIO, GPIO, JTAG	,
IEEE 1588 PTP	· ·	PCI-SIG SR-IOV, 256 VF, 8 PF	,	,	PLDM, MCTP (SMBus or PCIe), RBT	,
.=== =====		264 port virtual switch	J	J	M.2 / U.2 connectors for DAS	,
Stateless Offloads		EVB, VEPA, Flex10, VNTag	,	,	SGMII for 1Gb BMC interconnect	,
TCP/UDP checksum offload for IPv4 & IPv6	~ ~	512 MAC addresses	J	J	MCTP over PCIe VDM	
TSO, LSO, and GSO for IPv4 & IPv6	· ·	NAT Offload	,	,	JTAG IEEE 1149.1 and IEEE 1149.6	
VLAN filtering, insertion & extraction	· ·	Will Official	•	•	G.8273.2 Class C high-accuracy boundary clock	,
Packet filtering and attack protection	· ·	Streaming			SyncE	
Nanosecond granularity 64b timestamping	, ,	Integrated Traffic Management	J	J.	Synce	• •
Ethernet Routing (packet header rewrite)	, ,	Advanced QoS support	J	J	Boot Facilities	
Packet Tracing and Packet Sniffing	, ,	Hierarchical QoS	J	Ĵ	iSCSI, PXE, UEFI	.
Adaptive interrupt coalescing	V V	The tarefficult Q00	•	~	Secure Boot	∓ ¥ ن
mapare interrupt coalestillg	V V	High Performance RDMA			Secure Door	÷ •
Receive side scaling (RSS)	• •	IIIBII I EITOITIIAIICE NDIVIA				
Receive side scaling (RSS)		Native RoCEv2 support				
Receive side scaling (RSS)		Native RoCEv2 support Native iWARP support	y	,		

Ordering Information

	T7ASIC	N7ASIC
Memory	Optional	Optional
Package Size (0.8mm pitch)	31mm	31mm
400Gb Typ Power*	19-33W	21-29W
400Gb WC Power*	22-37W	24-31W
200Gb Typ Power*	11-22W	11-17W
200Gh WC Power*	14-26\M	17-23\\/

^{*} Configuration dependent

Physical & Environmental

- Fully RoHS Compliant
- Operating Temp: -40° to 55° C or -40° to 131° F
- Operating Humidity: 5 to 95%

Chelsio Communications www.chelsio.com sales@chelsio.com +1-408-962-3600

Applications

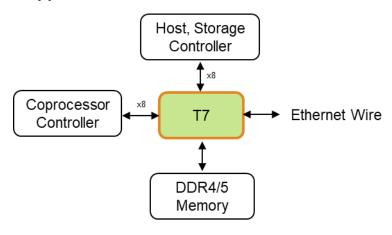


Figure 1 – Generalized Bridge

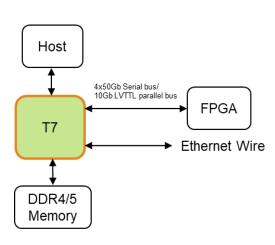


Figure 2 – iNIC Application

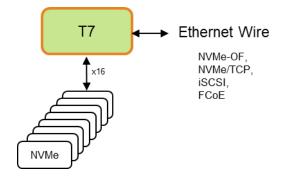


Figure 3 - NVMe-Ethernet Bridge

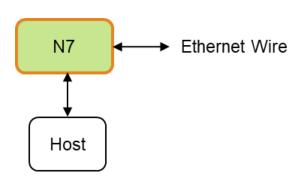


Figure 4 - Legacy Application



Figure 5 - NVMe-NVMe Bridge

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH CHELSIO PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN CHELSIO'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, CHELSIO ASSUMES NO LIABILITY WHATSOEVER, AND CHELSIO DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND OR USE OF CHELSIO PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. CHELSIO PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS. CHELSIO MAY MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE.

Copyright © 2024 - Chelsio Communications - All rights reserved.

Chelsio Communications <u>www.chelsio.com</u> <u>sales@chelsio.com</u> +1-408-962-3600