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CHELSIO WIDENS SMARTNIC LEADERSHIP WITH PIONEERING 7TH GENERATION UNIFIED WIRE

T7 DPU Family Accelerates a Wide Range of Storage, Networking, and Security workloads Supported by Modern Storage, Enterprise, and Cloud Applications

SUNNYVALE, CA – April 27, 2022– Chelsio Communications, Inc., a leading provider of high performance (1/2.5/10/25/40/50/100/200/400Gb) Ethernet Unified Wire Adapters and ASICs for storage networking, virtualized enterprise datacenters, cloud service installations, and cluster computing environments, today introduced its new 7th generation Unified Wire DPU product family architected to support and accelerate a wide range of networking, storage and security workloads supported by modern enterprise and cloud datacenter applications.

The dramatic migration to hybrid clouds, multifaceted security requirements, and proliferation of modern applications, such as artificial intelligence/machine learning (AI/ML), have accelerated the demand for highly efficient programmable data-centric processing and storage architectures. By combining high-performance and low-power compute with industry-leading seventh-generation data-path acceleration, the Chelsio T7 DPU family provides a significant ROI benefit through addressing inefficiencies due to overprovisioning of data center compute, networking, and storage resources.

Offering four times the bandwidth compared to previous generations of Unified Wire, the T7 DPU family incorporates up to eight Arm Cortex A72 cores for out-of-the-box support of embedded applications for control path processing, seventh generation Very Large Instruction Word (VLIW) processor for storage, networking, and security protocol processing at up to 400Gb, using 56Gb PAM4 SerDes. It also integrates PCIe 5.0 x16 with the ability to be either

Root Complex and/or End Point, a PCIe switch and an Ethernet switch. The Arm cores are primarily intended for use by the user since the embedded 400Gb core and multiple RISC engines will handle the standard protocol processing and offload activities. As such, the T7 DPU provides a considerably higher level of functionality at a lower power dissipation than traditional DPUs that are only based on embedded RISC cores.

T7 DPU supports all the host software of its predecessors, T5 & T6, as-is, thus enabling customers to leverage all prior software investment. It also supports all the features of T5 & T6, and, in addition, adds hardware-based acceleration for RoCEv2, compression, dedupe, erasure coding, root of trust, as well as a variety of other features. With the single chip iWARP/RoCEv2 implementation that can handle high capacity all-to-all traffic for large clusters, T7 is expected to provide a solid fabric replacement for InfiniBand for GPU clusters or HPC installations. The scalability of Chelsio's T7 DPU architecture will continue to meet the upcoming speeds of Ethernet and future generations of Terminator, and thus the portability and preservation of the software investment are both assured.

T7 has evolved the Terminator architecture to enable the full suite of offloads using the host memory with high capacity while caching a subset of the connections in hardware, and as such removes the need for card memories, thus enabling the single chip server/cloud side instantiations of T7 to run the exact same software as the target/appliance side of the wire with high capacity. The unique data-flow architecture of the T7 DPU further allows adjusting the clock rates to match the power dissipation to the required workload.

With T7 DPU, Chelsio also enters the computational storage market where on-the-fly compression and encryption increases the effective density of SSD drives. In addition, the native NVMe-NVMe and NVMe-Ethernet bridging function capabilities enable support for a single chip solution to support a full suite of storage protocols such as RAID along with the standard networking functions.

T7 further provides a native ability to integrate seamlessly with FPGAs, and thus provides a flexible platform where an arbitrary task can be decomposed to its parts and run on the offload engines, VLIW engine, FPGA, Arm cores, embedded RISC engines or the host drivers.

"T7 has several confirmed OEM wins already in the cloud, storage, server space, and represents a quantum jump in the level of functionality of our products and provides a generalized solution that can fully address the challenges of efficient data processing and movement across cloud to storage with the confidence of having several generations of offload products in production," stated Kianoosh Naghshineh, CEO at Chelsio Communications. "T7 ASIC now addresses the Smart NIC, D7 ASIC addresses Computational Storage, and S7 ASIC addresses generic server markets. T7 DPU thus significantly expands Chelsio's total addressable market and provides a platform and tools to enable Chelsio's software and solution partners to address several verticals. This collaboration to bring value added products to market together with our software and solution partners is something that we remain very committed to."

"Robust cutting-edge cloud applications require a new underlying data center infrastructure," said Greg Schulz, Sr. Analyst Server StorageIO. "Chelsio T7 DPU is a new type of I/O processor optimized to process data-centric workloads offloading server CPU overhead of software-defined networking, storage, security and other cloud-native services while boosting application performance."

T7 DPU Models

T7 DPU family is manufactured in TSMC 12FFC process and comprises the following models:

- T7 ASIC, 31mm package, full suite of features, with optional external memories
- S7 ASIC, 21mm package, server offload features, without requiring external memories
- D7 ASIC, 21mm package, full suite of features, without requiring external memories

T7 DPU products are undergirded by more than 2 decades of offload products shipped to enterprise customers and by several existing or in progress US patents, such as: 7831745,

7945705, 7616563, 8139482, 8339952, 8155001, 7724658, 7760733, 7715436, 8213427, 7660264, 8686838, 7924840, 7660306, 9537878, 8935406, 589587, 8356112, 8060644, 7826350, 7831720, 8122155, 8856947, 8621627, 9357003, 8886821, 8346919, 8873389, 8806154, 9628370, 9390056, 9413695, 9619245, 9444754, 9684597, 10681145, 9444769, 10225239, among others.

Availability

T7 DPU ASICs will be sampling in 4Q22 and similar to T5 and T6, are expected to be in production on first silicon within one quarter of samples. T7 DPU emulation platforms for software development are available to early access customers. Additional details and samples will be available at the full product launch in 4Q22. Please contact Chelsio for more information.

About Chelsio Communications

Chelsio is a recognized leader in high performance (1/2.5/10/25/40/50/100/200/400Gb) Ethernet adapters for networking and storage within virtualized enterprise datacenters, public and private hyperscale clouds, and cluster computing environments. With a clear emphasis on performance and delivering the only robust offload solution, as opposed to simple speeds and feeds, Chelsio has set itself apart from the competition. The Chelsio Unified Wire DPU fully offloads all protocol traffic, providing no-compromise performance with high packet processing capacity, sub-microsecond hardware latency and high bandwidth. Visit the company at www.chelsio.com and follow the company on Twitter and Facebook.

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