CORE IP With PCIe Interface

Chelsio Terminator Core IP

High Performance Converged Ethernet Interface Engine

Specifications

- High performance packet and protocol processor with complete software suite
- Multiple Ethernet ports
- Configurable port speed 10/25/40/50/100 Gb
- PCI application layer system interface
- Complete stateless offload suite
- Complete full offload suite (TCP, UDP, iWARP, iSCSI, FCoE, NVMe-oF)
- Full TLS/SSL, DTLS, IPsec, SMB 3.X crypto offload
- Flexible DMA engine
- Cut-through design
- Low memory usage
- Ultra low latency
- Flexible I/O virtualization support
- Network virtualization tagging
- Independent virtual interfaces
- Optional integrated edge switch
- SDN and OpenFlow
- L2/VLAN and L3/L4/L7 rules
- Network Function Virtualization
- Hardware Traffic management and QoS
- OVS Offload
- DPDK (Data Plane Development Kit)
- Integrated media streaming offload
- HW based firewall and NAT offload
- Traffic filtering & management

Applications

- General networking
- Storage networking
- High performance computing
- Network convergence
- Distributed systems
- Cloud installations
- Virtualization and multi-tenant clouds
- Traffic monitoring and network security
- WAN optimization

Advantages

- Low risk, silicon proven IP
- Performance leadership
  - High bandwidth
  - High packet processing rate
  - Low latency
- Comprehensive feature set
- Highly efficient in area and power

Key Statistics

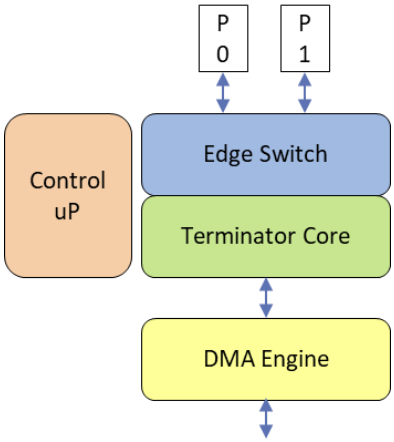
- High packet pipeline processing capacity
- Less than 800nsec latency at 500MHz for full (TX+RX) processing path
- Single pipelined engine design
- No dependency on traffic pattern
- No dependency on number of connections
- Microcode and Firmware programmable
- Edge switch with 140 virtual interfaces and broadcast/multicast support
- v-switch at line rate with up to 1M matching rules supporting more than 200K updates/sec

Firmware

- Single firmware image for all protocols
- Open interfaces for adding support for different physical interfaces

Overview

Chelsio's Terminator Core IP is a configurable, high performance Ethernet packet processing engine with a full suite of software, suitable for a wide range of SoC network connectivity solutions. At the heart of the Terminator line of silicon proven Network Interface Card (NIC) controllers, Chelsio's Core architecture is designed for low latency, high capacity cut-through processing, minimum cycles per byte (CPB) and maximum memory efficiency.



Terminator Core is the culmination of more than a decade of expertise with high performance network protocol implementation, and six generations of field proven designs. It offers support for a complete suite of storage and high performance computing networking protocols. Integrating the Core in an SoC design provides a drop-in server grade Ethernet managed and hyper-virtualized network controller. An optional edge switch component provides flexible packet replication and switching, with access control support.

Unified Wire Convergence

The Terminator Core can be configured to offload a comprehensive set of net-working, storage and compute protocols, including a complete list of stateless server adapter features including:

- Large Send Offload (LSO) and Large Receive Offload (LRO)
- Checksum offloads for TCP/UDP over IPv4/IPv6
- CRC offloads for RDMA, FCoE and iSCSI
- Load balancing – RSS
- Drop/Steer/Route filters offload and NAT offload
- NVGRE/VXLAN/GENEVE offload
- Timestamping, sniffing, tracing and other NFV features

The Core can also be configured to support one or more of the stateful offloads:

- iSCSI offload with T10-DIX
- FCoE offload with T10-DIX
- iWARP RDMA over Ethernet
- NVMe-oF
- NVMe-TCP offload
- Inline crypto (TLS 1.2, TLS 1.3 and IPsec) for all offloads (TOE, iSCSI, iWARP, etc.)
- TCP/IP and UDP/IP sockets

Terminator Core Architecture

The Terminator architecture is a proven 7th generation design with superior scalability and performance characteristics. The architecture easily scales from 10Gbps to 100Gbps speeds, and at 1Gbps per 8MHz is highly power and clock rate efficient. It centers on a proprietary, deeply pipelined programmable data-flow processor, designed from the ground up for cut-through processing, without access to external memory. The unique architecture is protected by more than 25 patents covering the design, features and operation of the Terminator Core. With multiple high speed port connectivity and ultra-low latency, the Terminator Core eliminates bottlenecks that impede the scalability of SoC based distributed system architectures and cloud installations.

Core Interfaces

The Terminator Core architecture is highly integrated with a single system bus interface such as PCI on the host side, and one or more Ethernet ports on the network side. The system interface is used for both system memory access and the Core memory access. The Core can also be configured to utilize system memory to scale full offload protocols and flow state support.

The optional embedded edge switch allows forwarding traffic from host-to-host side, enabling v-switch offload in virtualized environments and from wire-to-wire port on the network side. The switch is SDN/OpenFlow compatible, and supports forwarding traffic based on L2-7 rules, providing switching, routing and application payload proxy functionality. The Core supports up to 1M matching rules and more than 200K updates/sec. It also implements header rewrite capabilities, which enable advanced functionality such as Network Address Translation (NAT) offload and Intrusion Detection Services (IDS).

A control processor module runs the Core firmware component, which handles the control path and management functions.

Software Support

Chelsio offers a full suite of protocol software drivers for all the major operating systems. See https://www.chelsio.com/support/ for the latest information.

Configuration Options

The Core IP can be configured with the following options:

- Multiple Ethernet side interfaces
- Connection capacity: 32 up to 1M
- Link speeds: 10G, 25G, 40G, 50G and 100G
- Embedded edge switch
- Protocol offload capabilities

Security

- AES 128/256 and SHA1/SHA2 offload
- TLS/SSL, DTLS, IPsec and SMB 3.X crypto support
- Full offload and lookaside co-processor modes

High Performance RDMA

- Low latency and line rate bandwidth
- Enhanced RDMA primitives including Atomics & Immediate data
- iWARP support
- Native support for Windows Server 2012-R2, 2016, 2019, Azure Stack, Storage Replica, Storage Spaces Direct, Client RDMA, SMB-Direct, Network Direct, Guest RDMA
- Support for iSER, NFS-RDMA, Lustre-RDMA, NVIDIA's GPU-Direct, Hadoop-RDMA

TCP/IP Full Offload

- Full TCP stack including IPv4 & IPv6
- Extensive RFC compliance, fully featured
- VLAN support up to 4096 VLAN IDs
- Load balancing and failover capabilities

UDP & Multicast Offload

- UDP Sockets API
- Low user-to-user latency
- Multicast replication on ingress or egress

iSCSI

- iSCSI initiator and target mode stack
- CRC32 offload generation verification
- iSCSI proxy switching based on SCSI CDB
- Full HBA offload
- T10 DIF/DIX support

FCoE

- Full FCoE offload (Initiator or Target)
- Open FCoE offload (Initiator)
- CRC32 offload generation & verification
- Ingress & Egress ACL (Access Control List)
- T10 DIF/DIX support

Stateless Offloads

- TCP/UDP IPv4/6 checksum offload
- TSO, LSO and GSO for IPv4 & IPv6
- VLAN filtering, insertion & extraction
- Line rate packet filtering and attack protection
- Nanosecond granularity 64b timestamping
- Ethernet Routing (packet header rewrite)
- Packet Tracing and Packet Sniffing

Ethernet

- IEEE 802.3bj (100 GbE over copper/backplane)
- IEEE 802.3ba (40/100 GbE)
- IEEE 802.3by (25 GbE)
- IEEE 802.3ae (10 GbE)
- IEEE 802.3az Energy Efficient Ethernet
- IEEE 802.1p Priority
- IEEE 802.1Q VLAN Tagging
- IEEE 802.1Qbg EVB/VEPA
- IEEE 802.1BR Bridge Port Extension
- IEEE 802.1Qau Congestion Notification
- IEEE 802.3x Flow Control
- IEEE 802.3ad Load-balancing & Failover
- Ethernet II and 802.3 encapsulated frames
- Multiple MAC addresses per interface
- Jumbo Frames up to 9.6 Kbytes

Solution

- Encrypted Core IP
- Verification environment
- FPGA SDK
- Integration guide
- Terminator data book
- Firmware interface specifications
- Register set specifications
- Software drivers for Linux, Windows, FreeBSD, ESXi, XenServer and macOS